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Including Conformal Dielectrics in Multipole-Accelerated Three-Dimensional Interconnect Capacitance Extraction

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1 Introduction

The self and coupling capacitances associated with intergrated circuit interconnect are becoming increasingly important in determining final circuit performance and reliability. However, accurate estimation of these capacitances involves analyzing innately three-dimensional structures generated by multiple layers of polysilicon or metal conductors, separated by conformal or space-filling dielectrics. The recent development of multipole-accelerated boundary-element methods for three dimensional capacitance extraction has made accurate analysis of very complex structures computationally inexpensive, but the method was not directly applicable to analyzing integrated circuit interconnect because multiple dielectrics were not included[1]. In this brief abstract, we describe the equivalent charge approach to analyzing structures with dielectric interfaces, and give computational results from using the method in the multipole-accelerated extraction program FASTCAP2.

2 Interface Charge Approach

To determine all the self and coupling capacitances of a structure with m conductors, the conductor surface charges must be computed m times, with m different conditions on the conductor potentials. Given the conductor potentials, the conductor surface charges can be computed by replacing the conductor-dielectric and dielectric-dielectic interfaces with surface charges, represented as $\sigma(x)$. Then in this equivalent free-space problem, $\sigma(x)$ is determined by insisting that it produce a potential which matches conductor potentials at conductor-dielectric interfaces, and satisfies normal electric-field conditions at the dielectric interfaces[2, 3].

To numerically compute σ, the conductor surfaces and dielectric interfaces are discretized into $n = n_p + n_d$ small panels or tiles, with n_p panels on conductor surfaces and n_d panels on dielectric interfaces. It is then assumed that on each panel i, a charge, q_i, is uniformly distributed. For each conductor surface panel, an equation is written which relates the potential at the center of that i-th panel, denoted p_i, to the sum of the contributions to that potential from the n charge distributions on all n panels. Similarly, for each dielectric interface panel, an equation is written that relates the normal displacement-field difference at the center of that i-th dielectric interface panel to the sum of the contributions to that displacement field due to the n charge distributions on all n panels. The result is a dense linear system,

$$\begin{bmatrix} P \\ D \end{bmatrix} \begin{bmatrix} q \end{bmatrix} = \begin{bmatrix} p \\ 0 \end{bmatrix}, \qquad (1)$$

where $P \in \mathbf{R}^{n_p \times n}$ is a matrix of potential coefficients, $D \in \mathbf{R}^{n_d \times n}$ is the matrix representing the dielectric interface boundary conditions, $q \in \mathbf{R}^n$ is the vector of panel charges, and $p \in \mathbf{R}^{n_p}$ is the vector of conductor panel potentials.

In (1), the entries of the P-matrix are given by

$$P_{ij} = \frac{1}{a_j} \int_{panel_j} \frac{1}{\|x_i - x'\|}\, da'; \qquad (2)$$

where x_i is the center of the i-th panel and a_j is the area of the j-th panel. The off-diagonal entries of the matrix D are given by

$$D_{ij} = (\epsilon_b - \epsilon_a) \frac{\partial}{\partial n_i} \frac{1}{a_j} \int_{panel_j} \frac{1}{\|x_i - x'\|}\, da' \qquad (3)$$

and the diagonal entries are given by

$$D_{ii} = \frac{(\epsilon_b + \epsilon_a)}{2} \qquad (4)$$

where n_i is the normal to dielectric panel i, and ϵ_a and ϵ_b are the relative dielectric constants on the two sides of panel i.

3 Results from FASTCAP2

The dense linear system of (1) can be solved to compute panel charges from a given set of panel potentials, and the capacitances can be derived from the panel

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	1×1 bus	2×2 bus	3×3 bus	4×4 bus
cond. panels	252	792	1620	2736
dielec. panels	412	1192	2356	3904
total panels	664	1984	3976	6640
CPU minutes	0.9	7.7	35	88

Table 1: FASTCAP2 CPU times using an IBM RS6000/540

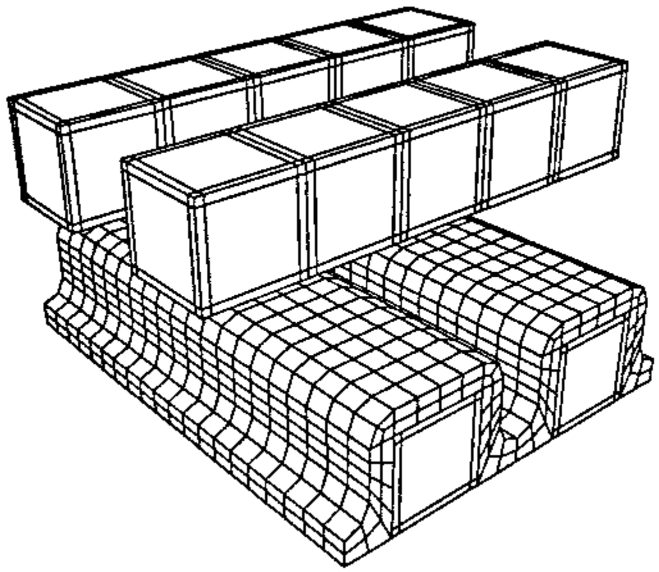

Figure 1: The 2×2 bus crossing problem with conformal dielectric.

charges. If Gaussian elimination is used to solve (1), the number of operations is order n^3. Clearly, this approach becomes computationally intractable if the number of panels exceeds several hundred. Instead, a generalized conjugate residual (GCR) algorithm is used to iteratively solve (1) and a multipole algorithm[4] is used to compute matrix-vector product required in each GCR iterate. Note that it is possible to use a multipole algorithm to perform the matrix-vector product because the surface charge formulation for the multiple dielectrics problem implies that the matrix-vector product is equivalent to computing the potential or electric field at n evaluation points due to n panel charges.

To determine the effectiveness of this approach, the multipole accelerated iterative algorithm was implemented in FASTCAP2, and tested on the easily parameterized conformally coated bus structure given in Figure 1. The CPU times required to analyze a 1×1 through 4×4 bus structure using FASTCAP2 are given in Table 1. For these experiments, the dielectric constant for the conformal coating on the lower conductors was 7.5 times larger than the permittivity of the surrounding insulator.

4 Conclusions and Acknowledgements

As is clear from Table 1, FASTCAP2 can rapidly analyze complex interconnect structures with conformal dielectrics in under an hour on a scientific workstation. Future work will focus on improving the efficiency of our preliminary implementation.

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