

Simulation and Modeling of the Effect of Substrate Conductivity on Coupling Inductance

Y. Massoud J. White

Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology
Cambridge, MA 02139.

Abstract

The goal of this work was to extend the FASTHENRY 3-D inductance extraction program to include the finite conductivity of a semiconductor substrate, and then use the modified program to investigate a variety of on-chip inductive effects. In addition, the limitations of a simple two-loop model for estimating coupling inductance is examined.

1 Introduction

It is commonly assumed that on-chip inductive effects are negligible, and this assumption is based on the presumption that the semiconductor substrate is a proximate ideal ground plane. For example, using the ideal ground plane assumption leads to a simple model for the coupling inductance between parallel interconnect lines. A pair of parallel lines of length l , with a separation distance y and height above the ground plane $\frac{1}{2}z$ can be represented, using the method of images, as the two loop structure shown in Figure 1. Two-dimensional analysis[2] of the structure leads to a simple formula for the coupling inductance,

$$L = \frac{\mu_0 l}{\pi} \ln \frac{\sqrt{y^2 + z^2}}{y}, \quad (1)$$

where l , z and y are the loop length, height and separation respectively, as defined in Figure 1. As is easily verified, equation (1) is accurate for the two-loop model when $l > y$.

In order to examine the accuracy of the ideal ground plane assumption, we extended the 3-D inductance extraction program FASTHENRY[1] to include finite conductivity volume ground planes. We then used that capability to more accurately model the semiconductor substrate and examine a variety of coupling effects. In the next section we briefly describe the FASTHENRY program and our modifications. In Section 3, we show

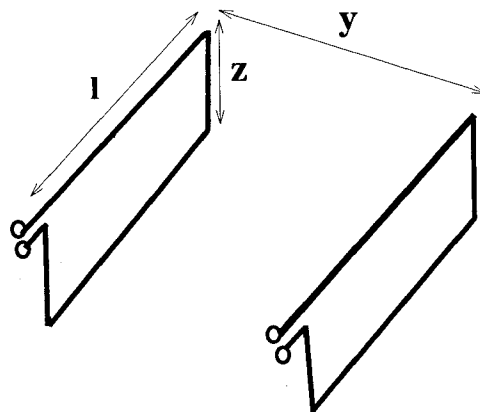


Figure 1: Simple two-loop coupling inductance model.

that the above two-loop model accurately predicts high-frequency coupling inductance, but on-chip and at frequencies below 20 gigahertz it is the much larger *low* frequency inductance that is important. In Section 4 we examine self-inductance and show it is also significant. Finally, conclusions and acknowledgments are given in Section 5.

2 Volume Discretization

FASTHENRY[1] uses a standard filament discretization of an integral formulation of magnetoquasistatic coupling[6]. The integral equation is

$$\frac{J(r)}{\sigma} + \frac{jw\mu}{4\pi} \int_{V'} \frac{J(r')}{|r - r'|} dv' = -\nabla\Phi(r), \quad (2)$$

where Φ is referred to as the scalar potential, and V' is the volume of all conductors.

Then, by simultaneously solving (2) with the current conservation equation,

$$\nabla \cdot J = 0, \quad (3)$$

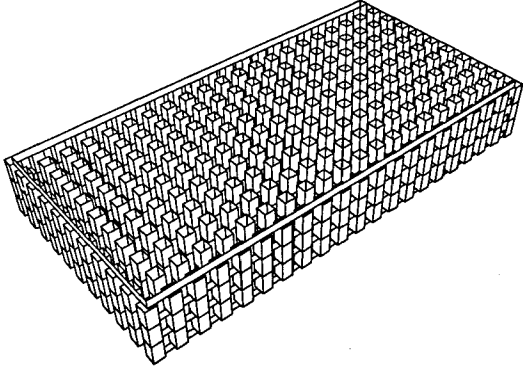


Figure 2: Example substrate volume filament-based discretization.

conductor current densities, J , and the scalar potential can be computed.

In FASTHENRY, a mesh formulation of the discretized equation is used to generate a dense system of equations which is solved iteratively using the fast multipole algorithm.

In order to examine the impact of the finite conductivity of the semiconductor substrate ground plane, a volume filament discretization[4] for the semiconductor substrate was added to the FASTHENRY program, as shown in Figure 2. The volume filament discretization for the substrate was constructed by first laying down a three dimensional grid of nodes, and then with filaments, connecting each node to its adjacent nodes excluding diagonally adjacent ones. Filament cross sections are chosen such that no space is left between parallel adjacent filaments.

3 Coupling Inductance

In this section, we examine the impact of the semiconductor substrate conductivity on coupling inductance. For the simulation examples below, the cross section of the conductors is 1μ by 1μ , reasonable for current DRAM technology[5]. The conductors were also chosen to be 100μ long, 1μ above the substrate, and have 2μ separation distance between them.

3.1 High and Low Frequency Limits

In Figure 3, the coupling inductance as a function of volume discretization is plotted for both very high and very low frequency. As is also shown in Figure 3, the formula based on the two-loop model accurately predicts the high frequency coupling inductance. For this comparison, the loop height z in equation (1) was set to twice

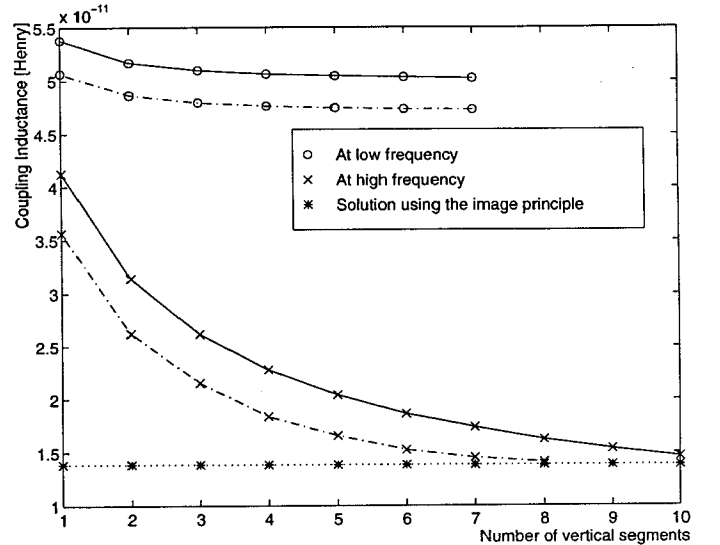


Figure 3: Convergence of the coupling inductance with discretization refinement. Solid line represents 30μ substrate thickness, and the dashed line represents 20μ substrate thickness. Note that the high frequency coupling inductance accurately matches that predicted by equation(1).

the distance to the substrate, based on the method of images approach[3].

The modified FASTHENRY program was also used to compute the coupling inductance as a function of frequency, for both realistic and idealized substrate conductivities. The results are plotted in Figure 4.

Note that the results in Figure 4 clearly indicates that with a semiconductor substrate ($10^{19}cm^{-3}$ doped silicon), and assuming operating frequencies below 20 gigahertz, it is the low-frequency-limit inductance, *not* the high-frequency-limit inductance, that is most important for predicting on-chip inductive coupling. Figure 4 also shows that the transition from low-frequency-limit inductance to high-frequency-limit inductance occurs at much higher frequency than 20 gigahertz for lighter doped silicon substrates. For instance, it occurs at 100 gigahertz for a $10^{17}cm^{-3}$ doped silicon substrate.

3.2 Comparison to Two-Loop Model

The two-loop model is inadequate for modeling the low-frequency-limit inductance. In Figure 5, it is shown that even by selecting a modified loop width, z , in the two-loop model of Figure 1, the model does not accurately predict parallel line inductive coupling over a range of conductor separations.

The simple model fails primarily because the low-

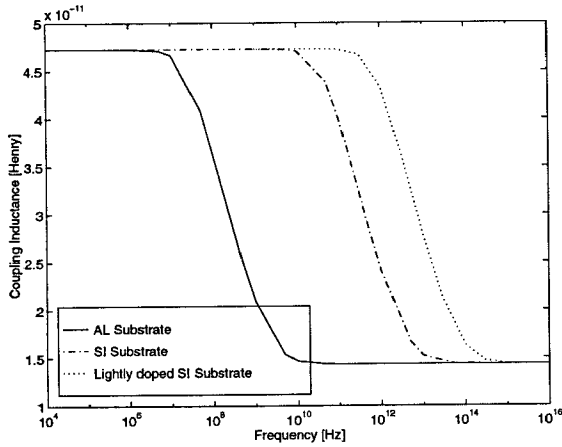


Figure 4: Inductance as a function of frequency for both an aluminum and semiconductor substrate. Same parameters as in Figure 3, with a substrate thickness of 20μ .

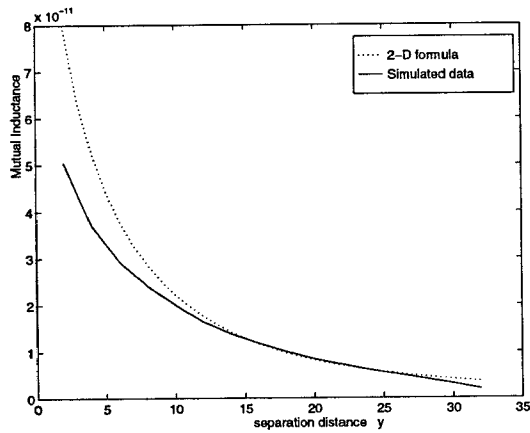


Figure 5: Comparison of the coupling inductance predicted by equation(1), and the simulated coupling inductance as a function of separation distance. Note that a “best-fit” loop height of 14.3μ was used for the comparison but the conductors are only 1μ above the ground plane.

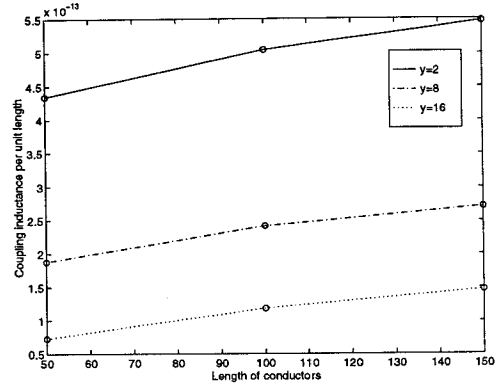


Figure 6: Inductance per unit length as a function of conductor length, for three different separation distances. Same conductor parameters as the example in Figure 4.

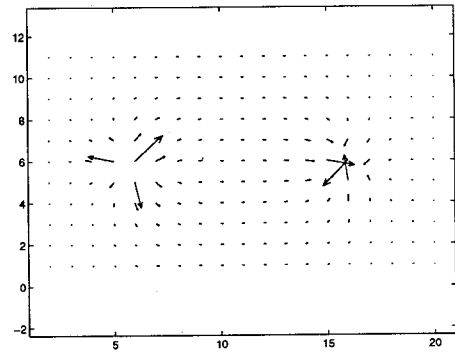


Figure 7: Typical low-frequency substrate surface current distribution.

frequency coupling inductance over a substrate ground plane is more three-dimensional in nature than can be modeled by a loop. This is demonstrated clearly in Figure 6, where the plots of inductance per unit length show a significant change with conductor length.

This three-dimensional behavior is due primarily to the current spreading from the contact points through the substrate, as shown in Figure 7.

3.3 Reducing Coupling Inductance

It is possible to reduce coupling inductance by using aluminum interconnect current return paths, rather than substrate return paths, as shown in Figure 8.

In order to significantly reduce the inductive coupling, the return paths must be very close to the original conductor, as shown in Figure 9. Figure 9 also shows that for a separation $y = 5\mu$, the coupling inductance when using an interconnect return path is always less than that of using a substrate return path as long as the dis-

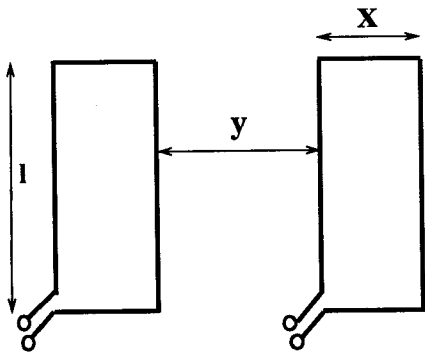


Figure 8: Returning path is through conductor rather than through the substrate

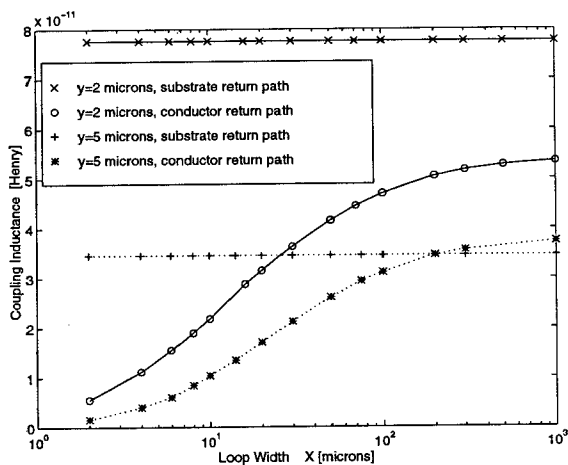


Figure 9: Coupling Inductance for both cases of conductor return path and substrate return path.

tance to the return path, x , less than 200μ . However, for $y = 2\mu$, the coupling inductance using an interconnect return path is always less than that of the substrate return path, irrespective of the value of the loop width x .

4 Self Inductance

It is possible to reduce coupling inductance without using nearby interconnect return paths by sufficiently separating the conductors. However, such an approach introduces another difficulty. This issue is loop self inductance, which can be comparable to loop self resistance. Table 1 shows that for the balancing frequency at which the self resistance balances the self inductance impedance is decreasing as the loop width, x , shown in Figure 8, increases. For instance, the balancing frequency is around 6 gighertz for a loop width of 25μ . Such frequencies are easily reached by the fast transitions in

high performance microprocessors, and therefore the self inductance of the loop can not be arbitrarily neglected.

x	Self Resis.	Self Induct.	Balancing Freq.
2μ	5.8Ω	0.06 nH	15.3 GHz
10μ	6.3Ω	0.13 nH	7.6 GHz
25μ	7.1Ω	0.19 nH	6 GHz
100μ	11.4Ω	0.37 nH	4.9 GHz

Table 1: Variation of the self impedance components and the balancing frequency with the loop width x .

5 Conclusions and Acknowledgments

In order to examine the accuracy of the ideal ground plane assumption we extended the 3-D inductance extraction program FASTHENRY to include finite conductivity volume ground planes. We then used that capability to more accurately model the semiconductor substrate and examine a variety of coupling effects. We showed that on-chip, and at frequencies below 20 gighertz, it is the much larger *low* frequency inductance that is important. In addition, we showed that self-inductance is also significant.

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