Simulation and Modeling of the Effect of Substrate Conductivity on Coupling Inductance and Circuit Crosstalk

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***Abstract*—The goal of this work was to simulate the effect of the finite conductivity of semiconductor substrates on the on-chip coupling inductance and then to investigate the effect of the on-chip coupling inductance on circuit crosstalk. In addition, the limitations of standard approaches for estimating coupling inductance are examined. A method for the reduction of the coupling inductance and its effect on circuit crosstalk is also discussed.**

***Index Terms*—Crosstalk noise, inductance, inductive coupling, substrate.**

I. Introduction

IT IS COMMONLY assumed that on-chip inductive effects are negligible and this assumption is based on the presumption that the semiconductor substrate is a proximate ideal ground plane. For example, consider a pair of parallel interconnect lines over a semiconductor substrate driving two inverters, as shown in Fig. 1. Using the ideal ground plane assumption leads to a simple model for the coupling inductance between parallel interconnect lines. The pair of parallel lines of length l, with a separation distance y and height above the ground plane $(1/2)\,z$ can be represented, using the method of images, as the two loop structure shown in Fig. 2. Two-dimensional (2–D) analysis [1] of the structure leads to a simple formula for the coupling inductance

$$L \cong \frac{\mu_0 l}{\pi} \ln \frac{\sqrt{y^2+z^2}}{y} \tag{1}$$

where l, z, and y are the loop length, height, and separation, respectively, as defined in Fig. 2. As is easily verified, (1) is accurate for the two-loop model when $l > y$.

In order to examine the accuracy of the ideal ground-plane assumption, we extended the three-dimensional (3-D) inductance extraction program FastHenry [2] to include finite-conductivity volume ground planes. We then used that capability to more accurately model the semiconductor substrate and examine a variety of coupling effects. In Section II, we briefly describe the FastHenry program and our modifications. In Section III, we show that the above two-loop model accurately predicts high-frequency coupling inductance, but on-chip and at frequencies below 20 gHz, it is the much larger *low* frequency inductance that is important. In Section IV, simulation results show the effect of the inductive coupling on circuit crosstalk. In Section V, a method for the reduction of the coupling inductance is shown. In Section VI, we discuss the resulted reduction in the circuit crosstalk due to using the method discussed in Section V. Finally, conclusions are given in Section VII.

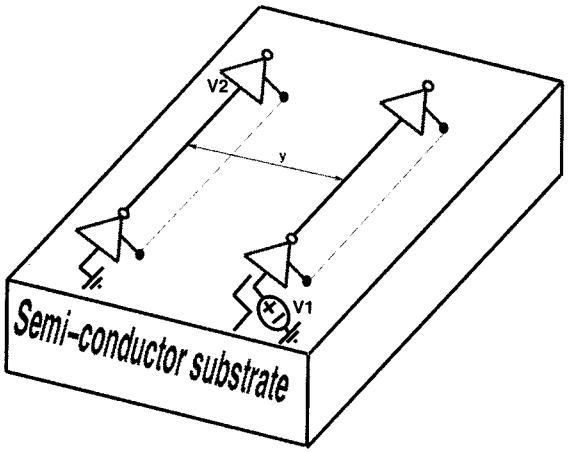

Fig. 1. Two long interconnect lines running over a semiconductor substrate.

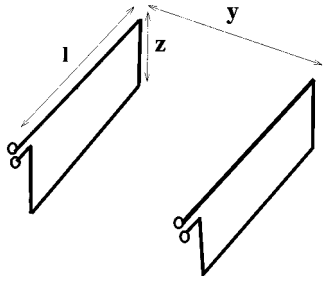

Fig. 2. Simple two-loop coupling inductance model.

II. Volume Discretization

FastHenry [2] uses a standard filament discretization of an integral formulation of magnetoquasistatic coupling [3]. The integral equation is

$$\frac{J(r)}{\sigma} + \frac{jw\mu}{4\pi} \int_{V'} \frac{J(r')}{|r-r'|} dv' = -\nabla\Phi(r) \tag{2}$$

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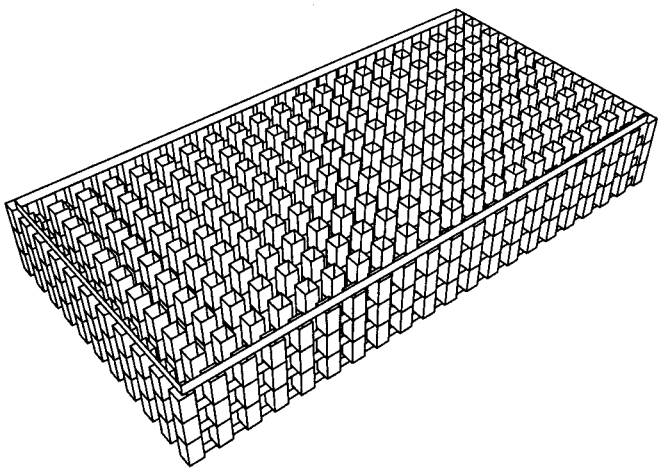

Fig. 3. Substrate volume filament-based discretization.

where Φ is referred to as the scalar potential, V' is the volume of all conductors, and J is the conductor current density.

Then, by simultaneously solving (2) with the current conservation

$$\nabla \cdot J = 0 \tag{3}$$

the conductor current densities and the scalar potential can be computed.

In FastHenry, a mesh formulation of the discretized equation is used to generate a dense system of equations which is solved iteratively using the fast multipole algorithm. In order to examine the impact of the finite conductivity of the semiconductor substrate ground plane, a volume filament discretization [4] for the semiconductor substrate was added to the FastHenry program, as shown in Fig. 3. The volume filament discretization for the substrate was constructed by first laying down a 3–D grid of nodes and then with filaments, connecting each node to its adjacent nodes excluding diagonally adjacent ones, as shown in Fig. 4. Filament cross sections are chosen such that no space is left between parallel adjacent filaments.

III. Coupling Inductance

In this section, we examine the impact of the semiconductor substrate conductivity on coupling inductance. For the simulation examples below, the cross section of the conductors is 1 μ by 1 μ, reasonable for current technologies. The conductors were also chosen to be 1000 μ long, 1 μ above the substrate and have 1 μ separation distance between them.

A. High- and Low- Frequency Limits

In Fig. 5, the coupling inductance as a function of volume discretization is plotted for both very-high and very-low frequency. As it is also shown in Fig. 5, the formula based on the two-loop model accurately predicts the high-frequency coupling inductance. For this comparison, the loop height z in (1) was set to twice the distance to the substrate, based on the method of images approach, which assumes a perfect ground plane [5].

The modified FastHenry program was also used to compute the coupling inductance as a function of frequency, for both realistic and idealized substrate conductivities. The results are plotted in Fig. 6.

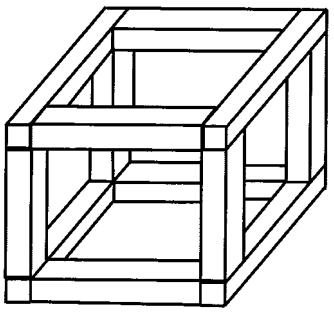

Fig. 4. A 2 x 2 x 2 substrate volume discretization to demonstrate how the filaments, in Fig. 3, are connected. Note that each filament represent a resistor in series with an inductor and also all the inductors are mutually coupled to each other.

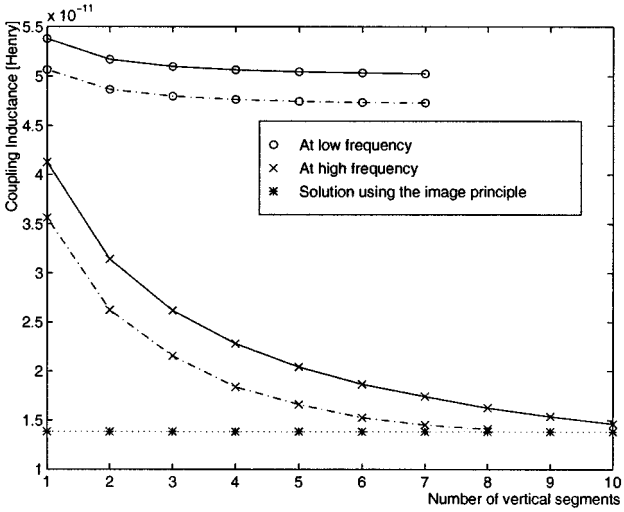

Fig. 5. Convergence of the coupling inductance with discretization refinement. Solid line represents 30 μ substrate thickness and the dashed line represents 20 μ substrate thickness. Note that the high frequency coupling inductance accurately matches that predicted by (1).

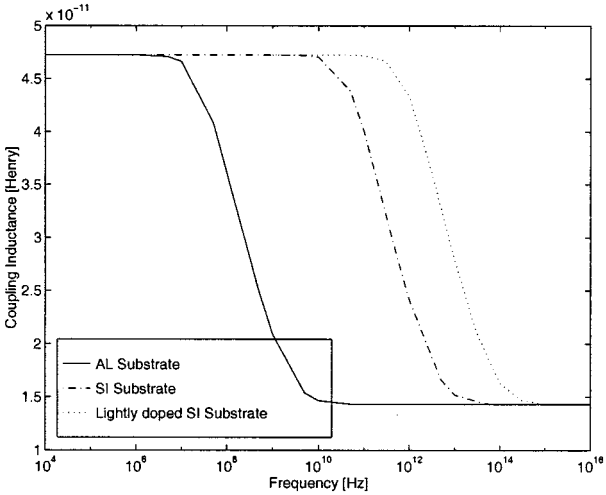

Fig. 6. Inductance as a function of frequency for both an aluminum and semiconductor substrate. Same parameters as in Fig. 5, with a substrate thickness of 20 μ.

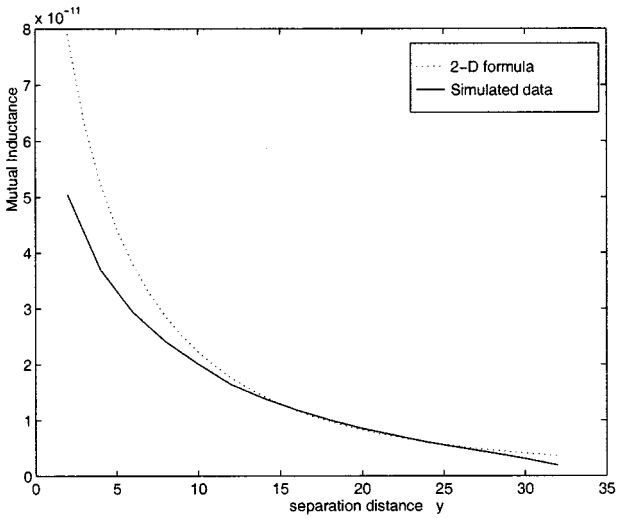

Fig. 7. Comparison of the coupling inductance predicted by (1) and the simulated coupling inductance as a function of separation distance. Note that a "best-fit" loop height of 14.3 μ was used for the comparison but the conductors are only 1 μ above the ground plane.

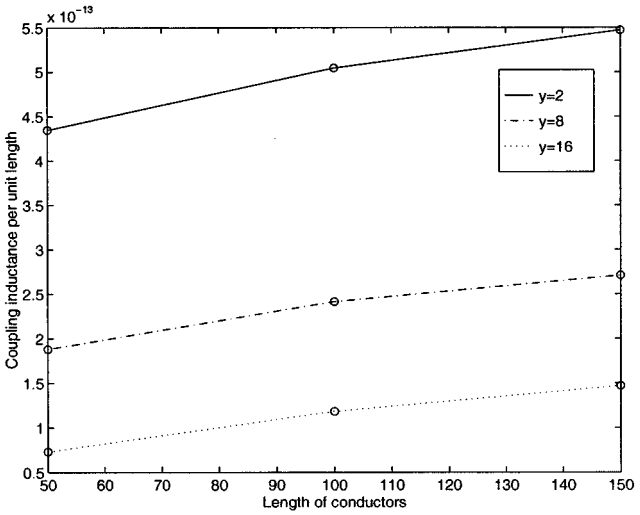

Fig. 8. Inductance per-unit length as a function of conductor length, for three different separation distances. Same conductor parameters as the example in Fig. 5.

Note that the results in Fig. 6 clearly indicates that with a semiconductor substrate (10^{19} cm^{-3} doped silicon), and assuming operating frequencies below 20 GHz, it is the low-frequency-limit inductance, *not* the high-frequency-limit inductance, that is most important for predicting on-chip inductive coupling. Fig. 6 also shows that the transition from low-frequency-limit inductance to high-frequency-limit inductance occurs at much higher frequency than 20 GHz for lighter doped silicon substrates. For instance, it occurs at higher than 100 GHz for a 10^{17} cm^{-3} doped silicon substrate.

B. Comparison to Two-Loop Model

The two-loop model is inadequate for modeling the low-frequency-limit inductance. In Fig. 7, it is shown that even by selecting a modified loop width, z, in the two-loop model of Fig. 2, the model does not accurately predict parallel line inductive coupling over a range of conductor separations.

The simple model fails primarily because the low-frequency coupling inductance over a substrate ground plane is more 3-D in nature than can be modeled by a loop. This is demonstrated clearly in Fig. 8, where the plots of inductance per unit length show a significant change with conductor length.

This 3-D behavior is due primarily to the current spreading from the contact points through the substrate, as shown in Fig. 9.

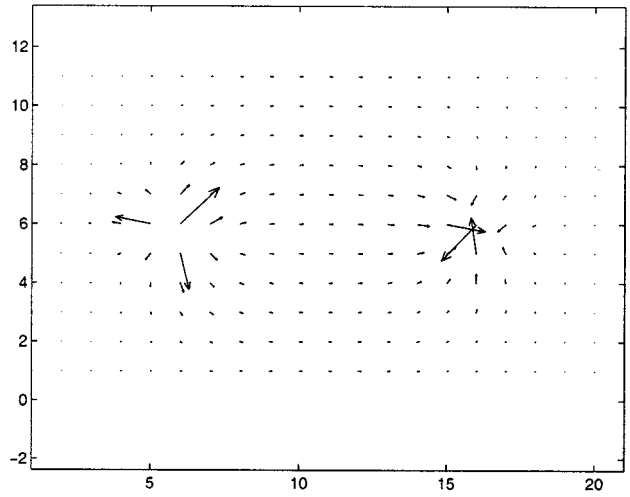

Fig. 9. Typical low-frequency substrate surface current distribution.

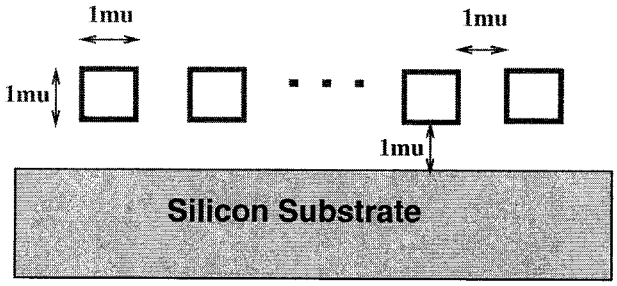

Fig. 10. A 16–bit data bus, running over 30 μ thick silicon substrate. Length of each line is 1000 μ.

IV. Crosstalk Simulations

In order to simulate the effect of the coupling inductance on circuit crosstalk, we ran our program on some examples. Consider 16 parallel 1000 μm aluminum interconnect data lines, where 15 of them are switching simultaneously, as shown in Fig. 10. Note that same kind of results can be produced for copper interconnects. Finer discretization may be needed for cladded copper lines [6].

We used a distributed RLC model to model the interconnects, where our program was used to model the resistances, the self inductances, and the coupling inductances. FastCap [7] was used to model the interconnect self capacitance to the substrate and the interconnect coupling capacitances. In order to test for the worst case crosstalk noise generated on the 16-bit data bus, we applied a 100 /s rise time step to all the inputs except the conductor in the middle. We also used simple buffers for drivers and receivers implemented using typical 0.25 μm technology devices and a 2.5 V supply. As shown in Fig. 11, a voltage glitch of more than 1 V appears at the end of the unswitched bus lines.

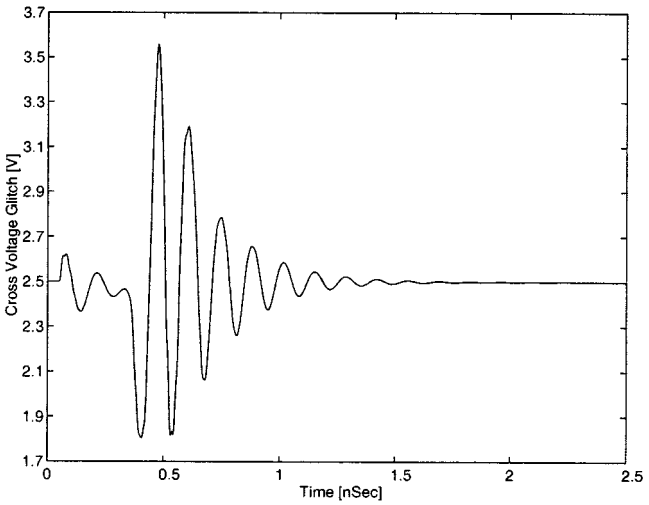

Fig. 11. Cross-coupled voltage glitch appears on the unswitched line due to the simultaneous switching of the other bits on the 16-bit data bus example. The original voltage before switching is 2.5 V.

Another example is a bus crossing structure consisting of two levels of four conductors, as shown in Fig. 12. The bus structure produces a voltage glitch of 0.6 V at the end of one line when the other seven conductors are simultaneously switching, as shown in Fig. 13.

V. Reducing Coupling Inductance

It is possible to reduce the coupling inductance by using interconnect current return paths, rather than substrate return paths, as shown in Fig. 14.

Fig. 15 shows that for a separation $y = 3\,\mu\text{m}$, the coupling inductance when using an interconnect return path is less than that of using a substrate return path as long as the distance to the return path, x, is less than 400 μm. However, in order to get a significant reduction in the coupling inductance, the return paths must be very close to the original conductor. For instance, to reduce the coupling inductance by a factor of 5, x should be less than 3 μm.

VI. Reducing Coupling Inductance Simulation Results

In order to verify this method of reducing coupling inductance and show its effect on circuit crosstalk, an example of eight parallel 1000 μm data lines is used. Fig. 16 shows the crosstalk voltage glitch that results on the middle unswitched line when other bits are simultaneously switching. It shows that the voltage glitch got reduced by a factor of 3 when every other line is grounded. This reduction in the crosstalk noise is as predicted in the previous section, since the return path is close to the original conductor. The cost of this crosstalk reduction strategy is that a total of 16 lines were used for the 8-bit data bus. The area used by the bus is therefore doubled. Fig. 17 shows that when grounding every third line, the total area of the bus has increased by 50% as a total of 12 lines were used and the crosstalk voltage glitch is reduced by a factor of 1.5. Fig. 17 also shows that the voltage glitch is only reduced by a factor of 1.25 when grounding every fourth line. Consequently, the farther the ground line is from the original conductor, the less significant the reduction of the crosstalk.

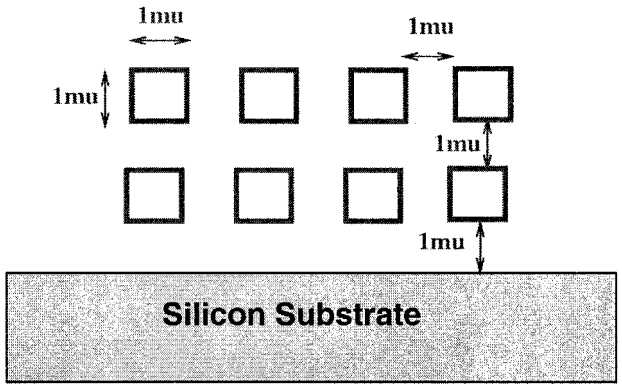

Fig. 12. Two levels of conductors, each level consists of four conductors. Length of each conductor is 1000 μ. The silicon substrate thickness is 30 μ.

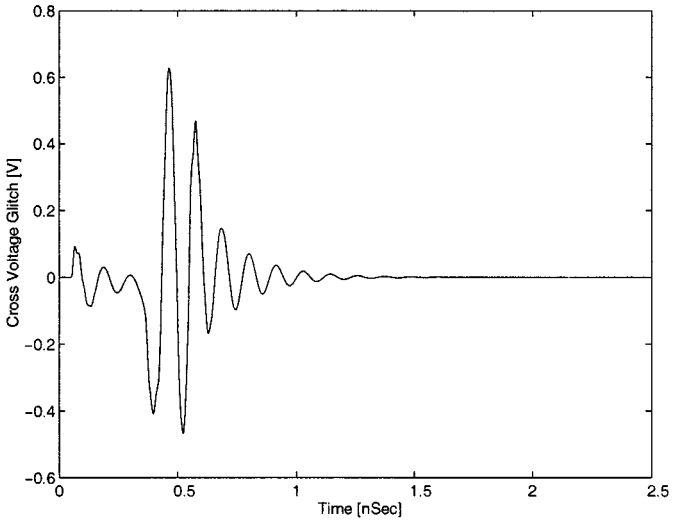

Fig. 13. Cross-coupled voltage glitch appears on the unswitched line due to the simultaneous switching of the other lines on the 2 x 4 bus example. The original voltage before switching is zero volt.

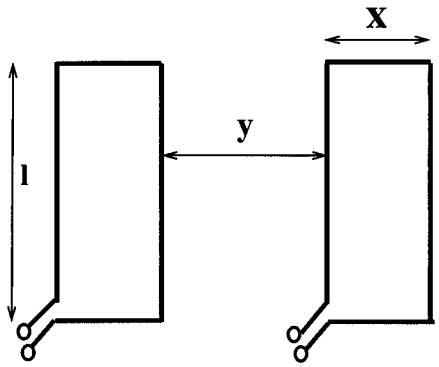

Fig. 14. Returning path is through conductor rather than through the substrate. $l = 100\,\mu$.

These simulation results show that coupling inductance can be reduced if interconnect current return paths are used rather than substrate return paths and that these return paths have to be very close to the original conductors. The cost for this coupling

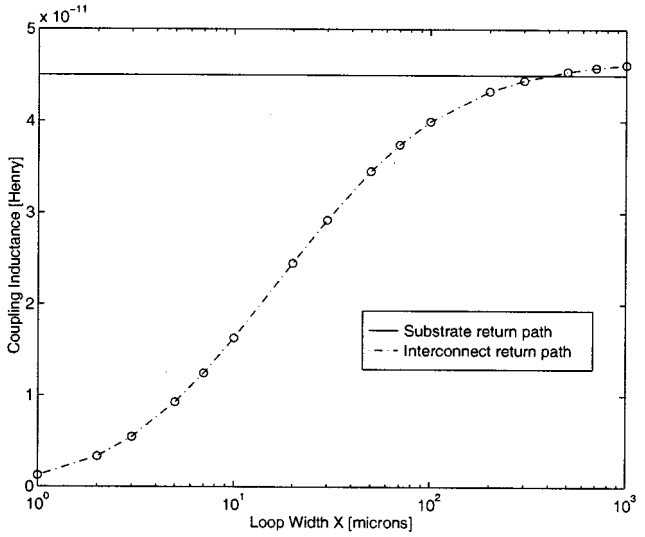

Fig. 15. Coupling inductance for both cases of conductor return path and substrate return path.

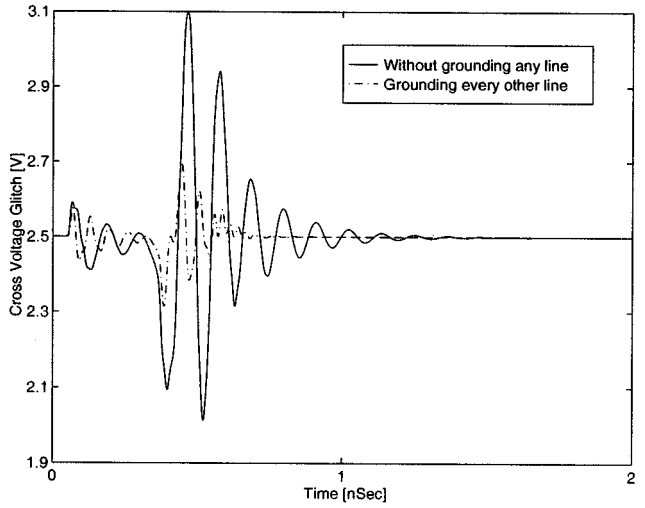

Fig. 16. Cross-coupled voltage glitch appears on the unswitched line due to the simultaneous switching of the other bits on the 8–bit data bus. It also shows the voltage glitch that produce when grounding every other line. Note that the area of the bus doubled as a total of 16 lines were used.

inductance reduction technique is that more ground lines will be used.

VII. Conclusion

In order to examine the accuracy of the ideal ground-plane assumption, we extended the 3-D inductance extraction program FastHenry to include finite conductivity volume ground planes. We then used that capability to more accurately model the semiconductor substrate and examine a variety of coupling effects. We showed that on-chip, and at frequencies below 20 GHz, it is the much larger *low*-frequency inductance that is important.

We also showed that coupling inductance can be reduced if interconnect current return paths is used rather than substrate return paths and that these return paths have to be very close to the original conductors.

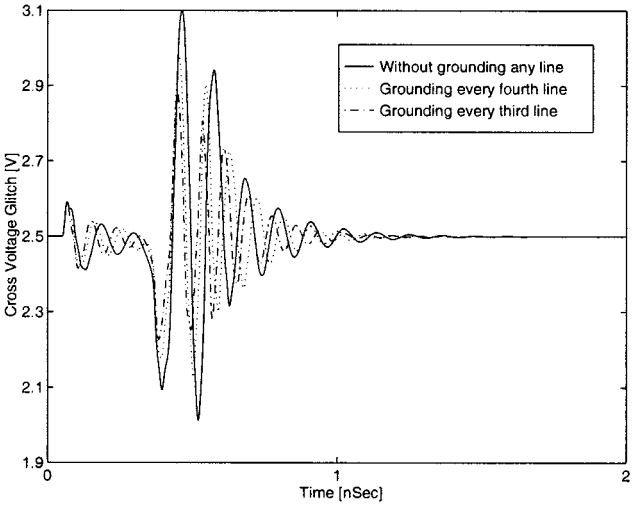

Fig. 17. Cross-coupled voltage glitch appears on the unswitched line due to the simultaneous switching of the other bits on the 8–bit data bus. It also shows the voltage glitch that produce when grounding every third line (a total of 12 lines used) or when grounding every fourth line (a total of 11 lines used).

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