Layout Techniques for Minimizing On-Chip Interconnect Self Inductance

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Abstract

Because magnetic effects have a much longer spatial range than electrostatic effects, an interconnect line with large inductance will be sensitive to distant variations in interconnect topology. This long range sensitivity makes it difficult to balance delays in nets like clock trees, so for such nets inductance must be minimized. In this paper we use two- and three-dimensional electromagnetic field solvers to compare dedicated ground planes to a less area-consuming approach, interdigitating the signal line with ground lines. The surprising conclusion is that with very little area penalty, interdigitated ground lines are more effective at minimizing self-inductance than ground planes.

1 Introduction

The potential for inductance to become a factor in the calculation of interconnect delay and signal integrity on deep submicron IC's has been forecast due to well known technology trends [1]. In high performance microprocessor design inductive effects have already begun to influence the design process [2]. With the rate of advancement in process technology continuing and market pressures for functional integration leading to larger chips, inductance may be expected to not only become a factor but a standard second order effect that designers must trade-off with other performance variables in the DSM space.

Today, most extraction and delay analysis tools are limited to RC networks leaving an inherent unpredictability in the design process where inductive effects are suspected. At the same time, typical design practices, based on RC analysis, of widening metal lines and increasing separation on critical nets to minimize delay, cross-talk, and skew are ineffective for reducing inductance. In this paper we use two-dimensional and three-dimensional electromagnetic field solvers to demonstrate a highly effective method for minimizing inductance without increasing die area. This approach can be used to help constrain a design to the RC domain to maintain predictability at some performance cost, or it can be used as a basis for alternative design rules where inductance and capacitance must be traded off to optimize for specific performance targets.

We start, in section two, by examining the inductance of a signal line sandwiched between ground return lines, and show that line spacing can have only a limited impact on self-inductance. In section three we use three-dimensional magnetoquasistatic analysis to show that for integrated circuit interconnect operating at below twenty-five gigahertz, it is the low frequency inductance that predicts performance[3]. In section four we compare the performance of the sandwiched structure, using two dedicated ground planes, and interdigitating thinned signal lines with thinned ground lines. Results in section four demonstrate that the interdigitated approach reduces self-inductance by more than a factor of four over the other techniques, for a modest rise in capacitance, resistance and area.

2 Two-Dimensional Self Inductance

The main focus of our study was coplanar clock trees, and as indicated in Figure (1), where the clock signal interconnect line is sandwiched between two ground return guard traces. We are using this typical structure to explore some methods for minimizing the self inductance, and therefore reduce the clock skew.

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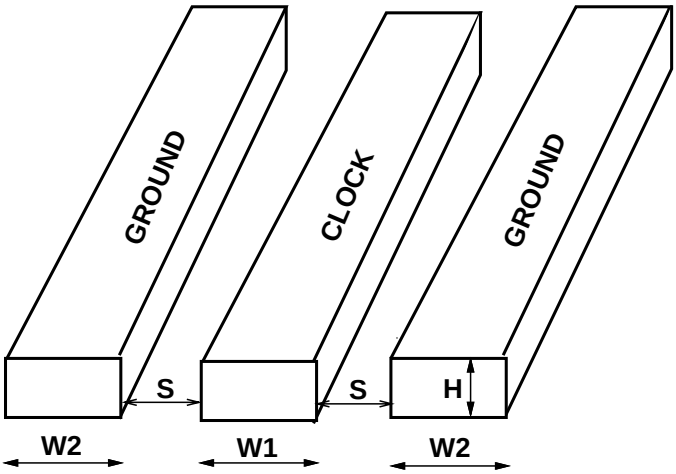

Figure 1: Coplanar Interconnect Clock Example

We used a two-dimensional field solver for the inductance and fixed the width of the clock signal line, W1, and the width of the ground return lines, W2, to 1um. As expected, we found that two-dimensional inductance is proportional to the separation distance between the clock signal line and the ground lines, S, as shown in Figure (2). Thus, in order to minimize the inductance, the separation distance between the clock signal line and the ground return lines, S, should be as small as possible. The two-dimensional inductance is calculated assuming high frequency meaning that fields exist only outside the conductors.

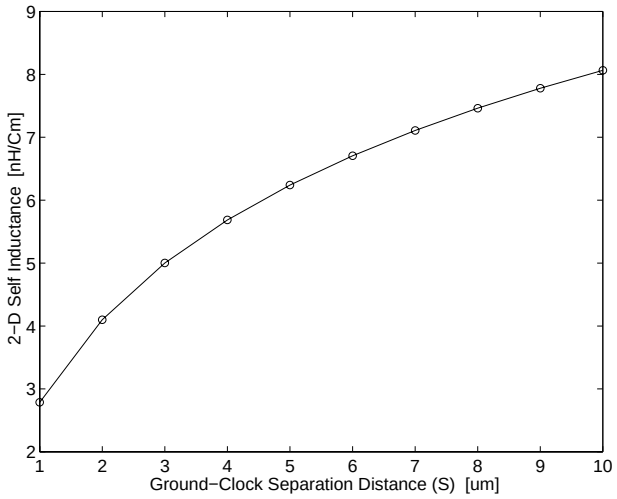

Figure 2: Variation of two-dimensional self inductance with the separation distance between the clock and the ground lines.

3 Three-Dimensional Self Inductance

It is often presumed, as was in the previous section, that near gigahertz clock rates imply that on-chip inductive effects can be analyzed by determining high frequency limit current distributions. In order to verify this assumption and get the specific frequency at which the conductors behave as perfect conductors, we did a frequency sweep on the inductance of the clock structure using the 3-D field solver FastHenry [4]. FastHenry employs multipole-accelerated Method-of-Moments techniques [5,6]. In Figure (3), we show the frequency dependence of the self inductance of the structure shown in Figure (1), where $W1 = W2 = S = 1\mu$. Note that the 2-D self inductance computed in the previous section is, as expected, the high frequency limit of the 3-D self inductance computed by FastHenry. Figure (3) also shows that for frequencies less than twenty-five gigahertz, it is the low-frequency self inductance not the high frequency self inductance that determines inductive effects. The corner frequency for self-inductance is determined by the

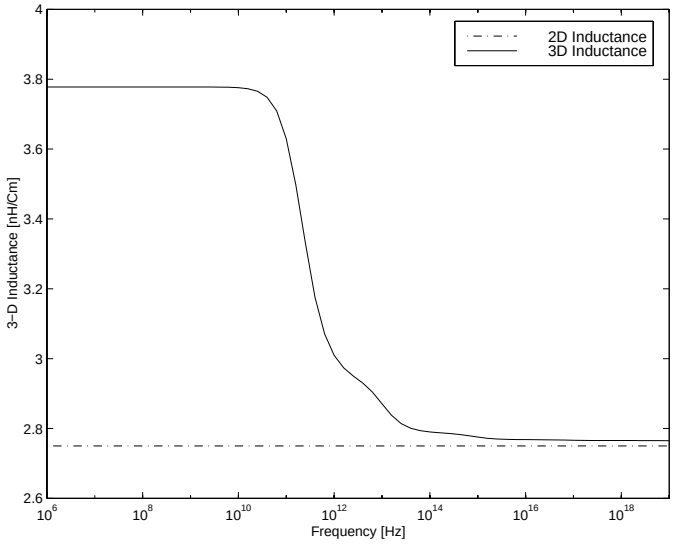

Figure 3: Three-dimensional self inductance frequency dependance for the clock structure in Figure (1). $W1 = W2 = S = 1\mu$.

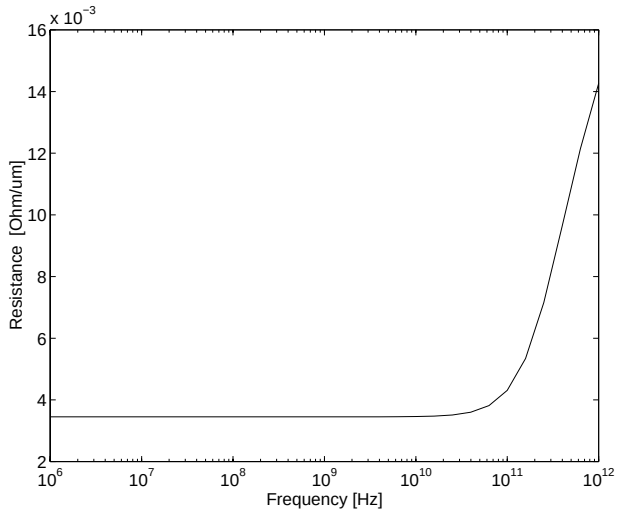

Figure 4: Resistance frequency dependance for the clock structure in Figure (1). $W1 = W2 = S = 1\mu$.

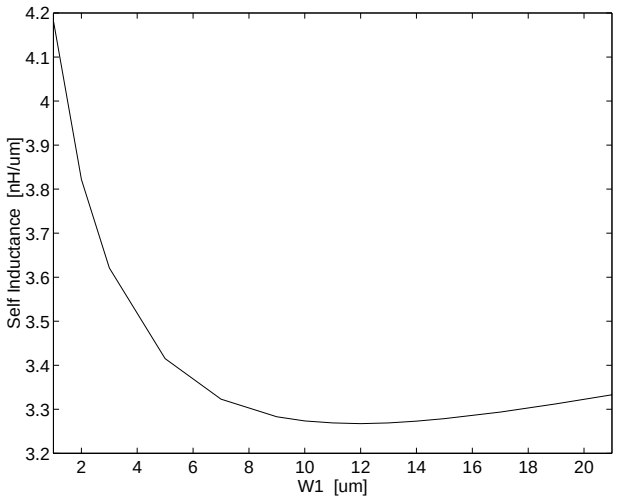

Figure 5: Variation of self inductance with W1 for the clock structure in Figure (1). $W2 = 3\mu, S = 1\mu$.

skin effect. The thinner the conductor is, the higher the corner frequency. Note that, in new technologies, conductor widths are getting to be much smaller than 1μ, and therefore the corner frequency is getting higher. This guarantees that the self inductance of interest is the low-frequency one. Figure (4) shows the frequency dependance of the resistance for the same structure. It shows that structure resistance has the DC resistance value for frequencies below the corner frequency and as frequency increases beyond the corner frequency, the resistance increases due to the skin effect.

4 Reducing Self Inductance

4.1 Optimizing Dimensions of Same Structure

In order to determine the optimum structure that minimizes the self inductance of the clock, we started by keeping the same structure in Figure (1) and trying to optimize its dimensions to reach minimum inductance. As shown in Figure (5), the inductance decreases as the width of the clock signal line, W1, increases, till it reaches a minimum value at $W1 = 12\mu$. After this minimum the inductance increases as W1 increases. The resistance of the clock is always decreasing as W1 is increasing as shown in Figure (6). This curve is not a linear function of W1 due to the constant resistance of the ground return lines, W2. The component of the total resistance from W1 continues to fall off linearly, but the total value saturates at the ground return value. The 3-D capacitance solver FastCap [7] was used to measure the structure capacitance. A floating plane was present to represent the density of a more realistic interconnect environment. Note that without including the floating plane, changes in capacitance between the conductors would be grossly over-estimated. Figure (7) shows that the capacitance is increasing linearly with W1.

Consider the two following structures, the first has $W1 = 3\mu$, $W2 = 3\mu$, and $S = 1\mu$, and the second has $W1 = 12\mu$, $W2 = 3\mu$, and $S = 1\mu$. The second structure has been optimized for minimum inductance given fixed $W2 = 3\mu$, its inductance is 10% less than the first structure. This 10% reduction in the inductance was achieved by using 2.3 times the original space, and 120% increase in the capacitance as shown in Figure (7).

Therefore, techniques for widening the clock to lower resistance, has little impact on the inductance. On the contrary, it might increase the capacitance significantly.

4.2 Using Dedicated Ground Plane Techniques

We also investigated using dedicated ground planes as return paths for the clock signal, as shown in Figure(8). Figure(9) shows the low frequency self inductance as a function of the ground plane width, Wg. Figure (9) also shows that, at around $Wg = 4\mu$, the inductance has a minimum value. After that minimum value, the low frequency self inductance increases monotonically as Wg increases. The current, at low frequency, is uniformly distributed on the ground plane, therefore, big current loops are formed when Wg is large. This increases the inductance. Figure(10) compares the self inductance frequency response of the dedicated ground planes case, with $W1 = H = Sg = 1\mu, Wg = 100\mu$,

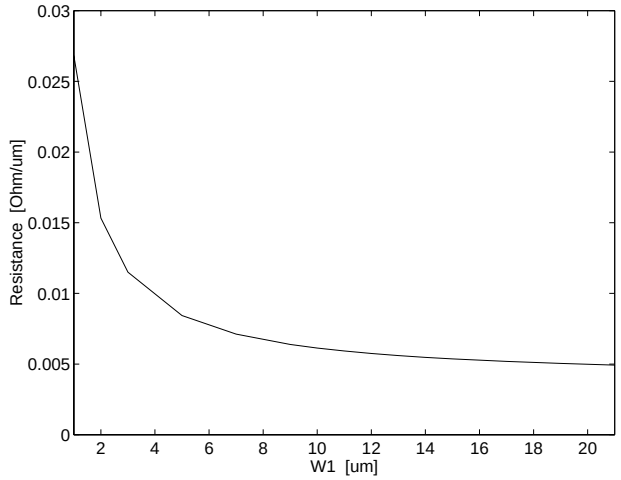

Figure 6: Variation of resistance with W1 for the clock structure in Figure (1). $W2 = 3\mu, S = 1\mu$.

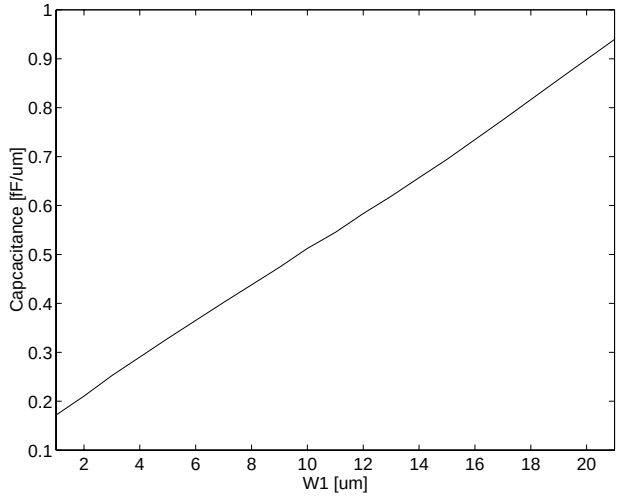

Figure 7: Variation of Capacitance with W1 for the clock structure in Figure (1). $W2 = 3\mu, S = 1\mu$.

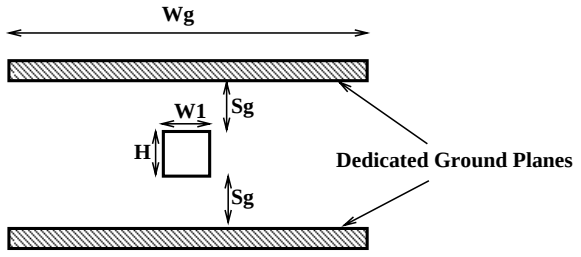

Figure 8: Using dedicated ground planes as return paths for the clock signal.

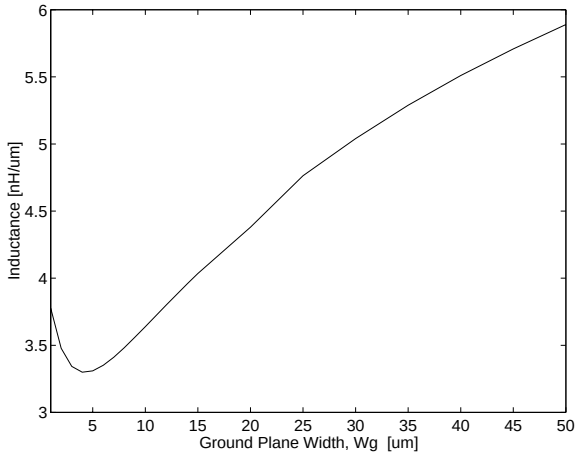

Figure 9: Self inductance for the structure shown in Figure(8). $W1 = H = Sg = 1\mu$.

and the two ground traces case, same as in Figure(3). Figure (10) also shows the frequency response when having both the ground traces and the ground planes as return paths. As shown in Figure (10), using only guard traces has the smallest inductance unless the frequencies of interest exceed several GHz. Above that frequency, dedicated ground planes have somewhat lower inductance, but since most of the energy in the signal is below several GHz, the use of dedicated ground planes is ineffective.

4.3 Using Interdigitated Techniques

As space is always a limiting factor for chip designs, it would be best if the inductance can be significantly reduced with only a limited increase of the total space allocated for the clock structure. In order to achieve that, one might think of distributing the clock signal on many lines, and doing the same for the ground return lines. As shown in Figure (11),

the 10μ signal line has been divided into two 5μ lines. Similarly, the two 3μ ground returns have been exchanged by three 2μ ground returns. This design resulted in no change in resistance, a 27% increase in capacitance, a 43% decrease in inductance, and only an 11% increase in area. The inductance is not reduced by 50%, as might be expected, due to the non-opposing mutual inductances.

We tried different interdigitated structures keeping the total structure width increase to less than 20%. Table (1) shows that a significant reduction of the self inductance of the clock can be achieved increasing the number interconnect lines in the clock structure. Table (2) shows the relative change in the RLC performance, for all structures.

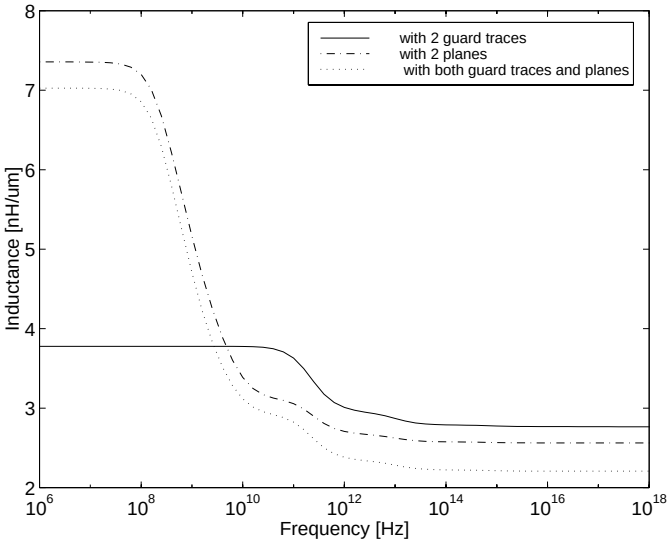

Figure 10: Self inductance Frequency response for the dedicated ground plane case shown in Figure(8), $W1 = H = Sg = 1\mu, Wg = 100\mu$, the guard traces case, as in Figure (3) , and both ground traces and ground plane case.

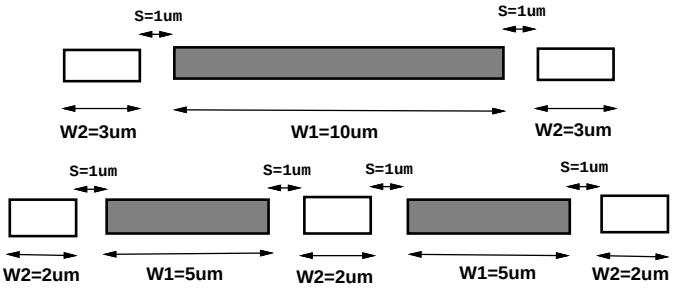

Figure 11: Interdigitated clock structure, using 5 lines instead of 3 lines. Total structure width has been increased from 18μ to 20μ.

N	W1	W2	Wt	R[$m\Omega/\mu$]	L[nH/Cm]	C[fF/μ]
3	10μ	3μ	18μ	R1=6.1	L1=3.273	C1=.5124
5	5μ	1μ	17μ	9.9	1.927	.6449
5	5μ	2μ	20μ	6.1	1.869	.6483
7	3μ	1μ	19μ	8.3	1.336	.7345
9	2μ	1μ	21μ	7.5	1.027	.8215
11	1μ	1μ	21μ	8.4	0.850	.8478

Table 1: Variation of the resistance, inductance and capacitance of the clock structure with the number of interconnect lines in the structure, N, and the total width of the clock structure, Wt. All lines are separated from adjacent lines by 1μ.

N	W1	W2	Wt	R/R1	L/L1	C/C1
3	10μ	3μ	18μ	1.00	1.00	1.00
5	5μ	1μ	17μ	1.62	0.59	1.26
5	5μ	2μ	20μ	1.00	0.57	1.27
7	3μ	1μ	19μ	1.36	0.41	1.43
9	2μ	1μ	21μ	1.23	0.31	1.60
11	1μ	1μ	21μ	1.38	0.26	1.66

Table 2: Relative Variation of the resistance, inductance and capacitance of the clock structure with the number of interconnect lines in the structure, N, and the total width of the clock structure, Wt. All lines are separated from adjacent lines by 1μ.

The resistance or the maximum space allowed for the clock, whichever is more critical in the design, determines the exact width for each line. As shown in Table (1), about the same reduction percentage in the inductance, can be achieved with two different 5 line structures. However, the five line structure with the 17μ wide clock structure has 62% more resistance than the 20μ wide clock structure. Table (2) also shows that the inductance can be reduced as low as 3.9 times by having the clock structure composed of 11 lines, where ground and signal lines are alternatively placed. This significant reduction in the inductance can be achieved with an insignificant increase in the total clock structure width, and clock resistance, and a modest increase in the capacitance.

5 Conclusions

In this paper we showed that for integrated circuit interconnect operating at below twenty-five gigahertz, it is the low frequency inductance that predicts performance. We then compared the performance of the sandwiched structure, using two dedicated ground planes, and interdigitating thinned signal lines with thinned ground lines. Our results demonstrate that the interdigitated approach reduces self-inductance by more than a factor of four over the other techniques, for a modest rise in capacitance, resistance and area.

6 Acknowledgments

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